Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A method for programming a PMOS single-transistor memory unit, said PMOS single-transistor memory unit being comprised of a silicon dioxide-silicon nitride-silicon dioxide (ONO) dielectric stack disposed on an N-well, a P type polysilicon gate disposed on said ONO dielectric stack, a P type doped source region disposed in said N-well at one side of said P type polysilicon gate, and a P type doped drain region disposed in said N-well on the other side of said P type polysilicon gate, the method comprising:

biasing said P type polysilicon gate of said PMOS single-transistor memory unit to a word line voltage V_{WL};

biasing said P type doped source region of said PMOS single-transistor memory unit to a source line voltage V_{SL} that is greater than the word line voltage V_{WL}, wherein

$|V_{WL}-V_{SL}|$

is larger than threshold voltage of said PMOS single-transistor memory unit, so as to provide an adequate gate-to-source bias to turn on a P-channel of said PMOS single-transistor memory unit;

biasing said P type doped drain region of said PMOS sin-

gle-transistor memory unit to a bit line voltage V_{BL}, wherein said bit line voltage V_{BL} is smaller than said source line voltage V_{SL}, so as to provide a lateral electric field for P-channel hot holes, wherein said lateral electric field forces said P-channel hot holes passing through said P-channel in an accelerated drift rate to said P type doped drain region, thereby inducing hot electrons near said P type doped drain region, and wherein some of induced hot electrons are injected into said ONO dielectric stack; and

biasing said N-well to a well voltage V_{NW}, wherein said well voltage V_{NW} is equal to said source line voltage V_{SL}.

[c2] 2.The method according to claim 1 wherein said hot electron injection occurs near said P type doped drain region, which is induced by channel hot holes, is referred to as "channel hot hole induced hot electron mechanism".

[c3] 3.The method according to claim 1 wherein said word line voltage V_{WL} is between 0~4V, said source line voltage V_{SL} is between 3~5V, said bit line voltage V_{BL} is 0V, and said well voltage V_{NW} is between 3~5V.

[c4] 4.The method according to claim 1 wherein said word line voltage V_{WL} is between -1~-5V, said source line voltage V_{SL} is 0V, said bit line voltage V_{BL} is between -

3~-5V, and said well voltage V_{NW} is between 0V.

[c5] 5.A method for programming a PMOS single-transistor memory unit, said PMOS single-transistor memory unit comprising a silicon dioxide-silicon nitride-silicon dioxide (ONO) dielectric stack disposed on an N-well, a P type polysilicon gate disposed on said ONO dielectric stack, a P type doped source region disposed in said N-well at one side of said P type polysilicon gate, and a P type doped drain region disposed in said N-well on the other side of said P type polysilicon gate, the method comprising:

biasing said P type polysilicon gate of said PMOS single-transistor memory unit to a word line voltage V_{WL}>0V;

floating said P type doped source region of said PMOS single-transistor memory unit; and

biasing said P type doped drain region of said PMOS single-transistor memory unit to a bit line voltage V_{BL} and biasing said N-well to a well voltage V_{NW}, wherein V_{NW}-V_{BL} bias>0V.

[c6] 6.The method according to claim 5 wherein said word line voltage V_{WL} is between 2~8V, said bit line voltage V_{BL} is -3~-6V, and said well voltage V_{NW} is between 0~5V.

[c7] 7.The method according to claim 5 wherein hot electron-hole pairs is generated at the junction between said

N well and said P type doped drain region, and wherein some of said hot electrons are injected into said ONO dielectric stack near said P type doped drain region through band-to-band tunneling (BTBT) mechanism.

[c8] 8.A method for reading a PMOS single-transistor memory unit, said PMOS single-transistor memory unit being comprised of a silicon dioxide-silicon nitride-silicon dioxide (ONO) dielectric stack disposed on an N-well, a P type polysilicon gate disposed on said ONO dielectric stack, a P type doped source region disposed in said N-well at one side of said P type polysilicon gate, and a P type doped drain region disposed in said N-well on the other side of said P type polysilicon gate, wherein electrons are localized in said ONO dielectric stack near said P type doped drain region, the method comprising:
biasing said P type polysilicon gate of said PMOS single-transistor memory unit to a word line voltage V_{WL};
biasing said P type doped source region of said PMOS single-transistor memory unit to a source line voltage V_{SL} that is smaller than said word line voltage V_{WL} ($V_{SL} < _{WL}$);
biasing said P type doped drain region of said PMOS single-transistor memory unit to a bit line voltage V_{BL} that is greater than said source line voltage V_{SL} ($V_{BL} V > _{SL}$); and
biasing said N-well to a well voltage V_{NW}, wherein said well voltage V_{NW} is equal to said bit line voltage V_{BL}.

[c9] 9.The method according to claim 8 wherein said word line voltage V_{WL} is 0V, said source line voltage V_{SL} is between -0.5~-2.5V, said bit line voltage V_{BL} is 0V, and said well voltage V_{NW} is between 0V.

[c10] 10.The method according to claim 8 wherein said word line voltage V_{WL} is 2.5V, said source line voltage V_{SL} is between 0~2V, said bit line voltage V_{BL} is 2.5V, and said well voltage V_{NW} is between 2.5V.

[c11] 11.A method for operating a PMOS single-transistor memory unit, said PMOS single-transistor memory unit being comprised of a silicon dioxide-silicon nitride-silicon dioxide (ONO) dielectric stack disposed on an N-well, a P type polysilicon gate disposed on said ONO dielectric stack, a P type doped source region disposed in said N-well at one side of said P type polysilicon gate, and a P type doped drain region disposed in said N-well on the other side of said P type polysilicon gate, wherein electrons are localized in said ONO dielectric stack near said P type doped drain region, the method comprising:
reading said PMOS single-transistor memory unit, comprising:
biasing said P type polysilicon gate of said PMOS single-transistor memory unit to a word line voltage V_{WL};
biasing said P type doped source region of said PMOS

single-transistor memory unit to a source line voltage V_{SL} that is smaller than said word line voltage V_{WL} ($V_{SL}<V_{WL}$); biasing said P type doped drain region of said PMOS single-transistor memory unit to a bit line voltage V_{BL} that is greater than said source line voltage V_{SL} ($V_{BL}>V_{SL}$); and biasing said N-well to a well voltage V_{NW}, wherein said well voltage V_{NW} is equal to said bit line voltage V_{BL};
erasing said PMOS single-transistor memory unit, comprising:
applying a negative erase voltage to said P type polysilicon gate of said PMOS single-transistor memory unit; and
applying a positive erase voltage to said N well of said PMOS single-transistor memory unit, thereby erasing said electrons localized in said ONO dielectric stack through Fowler-Nordheim tunneling mechanism.

[c12] 12.The method according to claim 11 wherein said word line voltage V_{WL} is 0V, said source line voltage V_{SL} is between -0.5~-2.5V, said bit line voltage V_{BL} is 0V, and said well voltage V_{NW} is 0V.

[c13] 13.The method according to claim 11 wherein said word line voltage V_{WL} is 2.5V, said source line voltage V_{SL} is between 0~2V, said bit line voltage V_{BL} is 2.5V, and said well voltage V_{NW} is 2.5V.

[c14] 14.The method according to claim 11 wherein said negative erase voltage is 6V.

[c15] 15.The method according to claim 11 wherein said positive erase voltage is +6V.